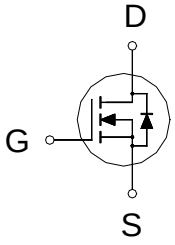
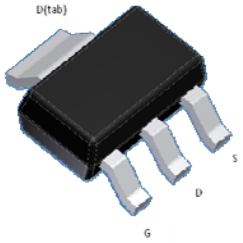
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	200V
$R_{DSON\ (MAX.)}$	0.5Ω
I_D	1.6A





UIS, 100% Tested

Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±30	V
Continuous Drain Current	T_C = 25 °C	I_D	1.6	A
	T_C = 100 °C		1	
Pulsed Drain Current[1]		I_{DM}	6.4	
Power Dissipation	T_C = 25 °C	P_D	6.25	W
	T_C = 100 °C		2.5	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		20	°C / W
Junction-to-Ambient	$R_{\theta JA}$		150	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_C = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	200			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	3.0	4.0	5.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 160V, V_{GS} = 0V			1	μA
		V_{DS} = 130V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	1.6			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 0.8A		0.4	0.5	Ω
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 0.8A		2		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		803		pF
Output Capacitance	C_{oss}			19		
Reverse Transfer Capacitance	C_{rss}			16		
Total Gate Charge[1,2]	Q_g	V_{DS} = 100V, V_{GS} = 10V, I_D = 0.8A		21.3		nC
Gate-Source Charge[1,2]	Q_{gs}			2.9		
Gate-Drain Charge[1,2]	Q_{gd}			6		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 100V, I_D = 0.5A, V_{GS} = 10V, R_{GS} = 6Ω		20		nS
Rise Time[1,2]	t_r			60		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			20		
Fall Time[1,2]	t_f			50		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				1.6	A
Pulsed Current[3]	I_{SM}				6.4	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.5	V

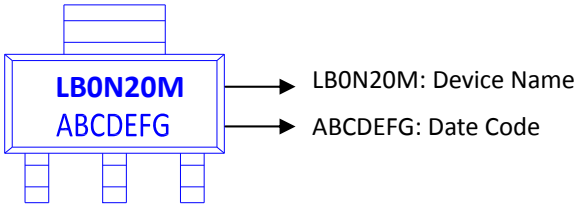
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

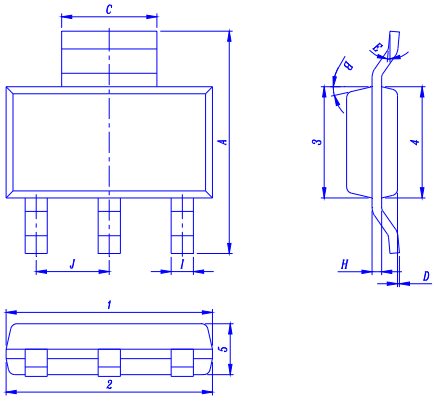
[3]Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: LB0N20M for SOT-223



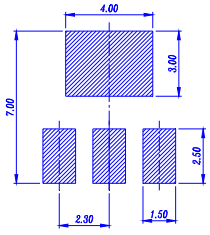
Outline Drawing



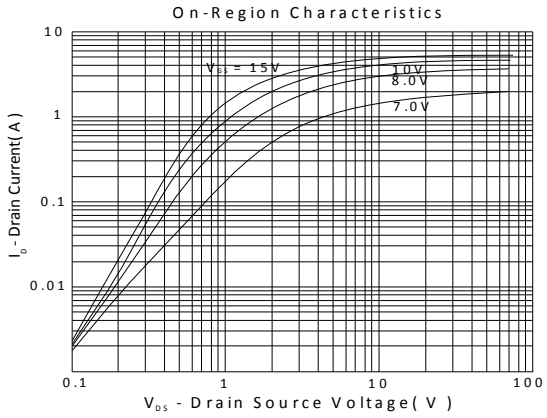
Dimension in mm

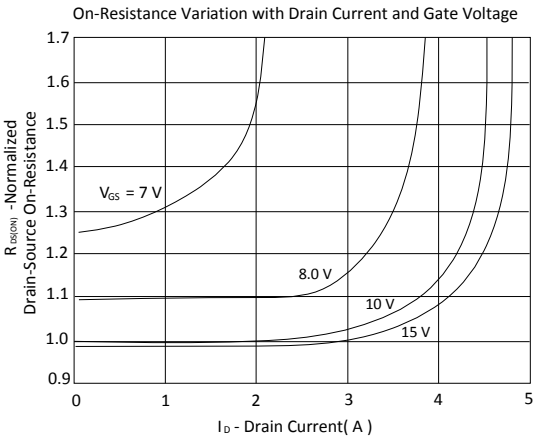
Dimension	A	C	D	E	I	H	B	J	1	2	3	4	5
Min.	6.70	2.90	0.02	0°	0.60	0.25			6.30	63.0	3.30	3.30	1.40
Typ.							13°	2.30					
Max.	7.30	3.10	0.10	10°	0.80	0.35			6.70	6.70	3.70	3.70	1.80

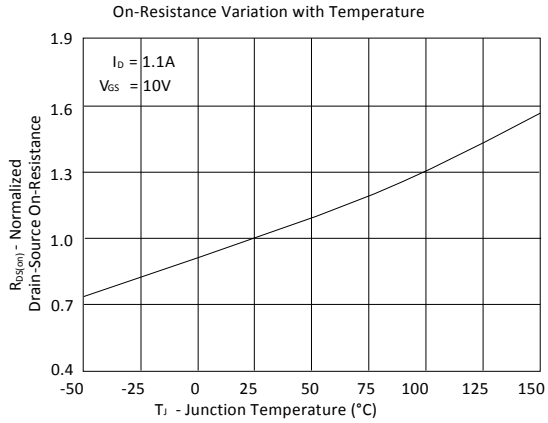
Recommended minimum pads

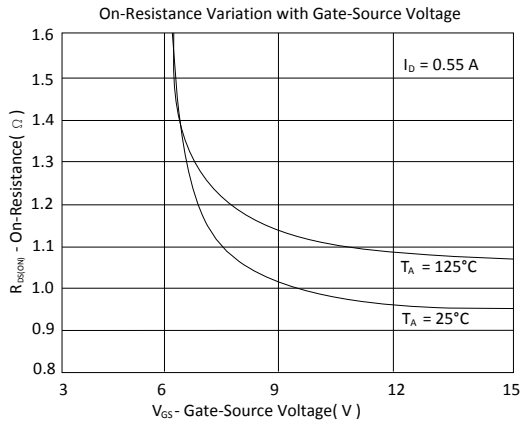


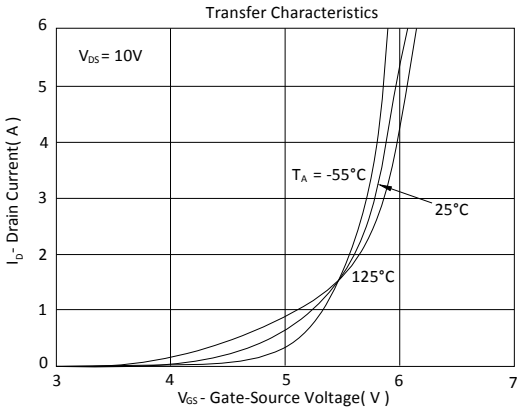
TYPICAL CHARACTERISTICS

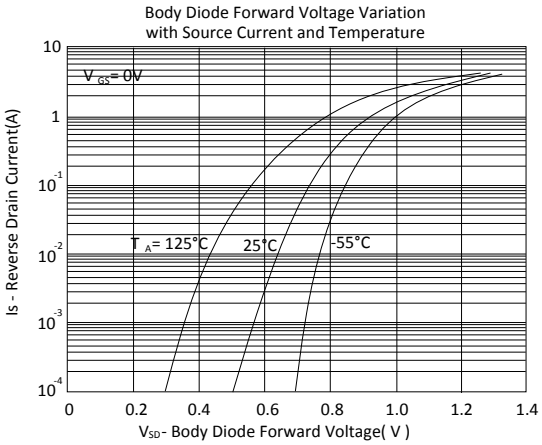




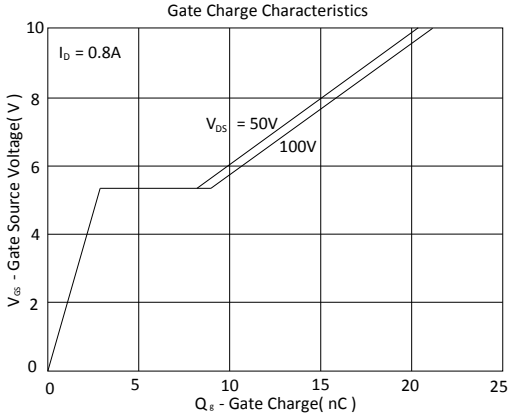




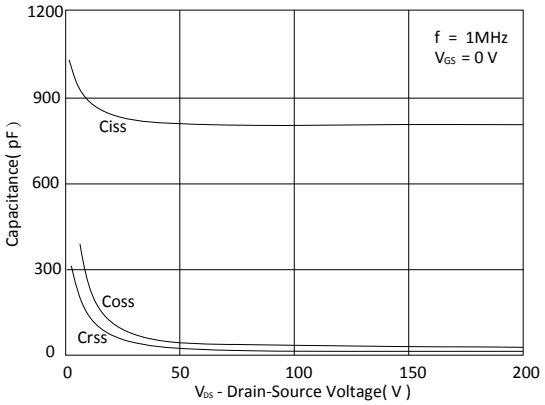




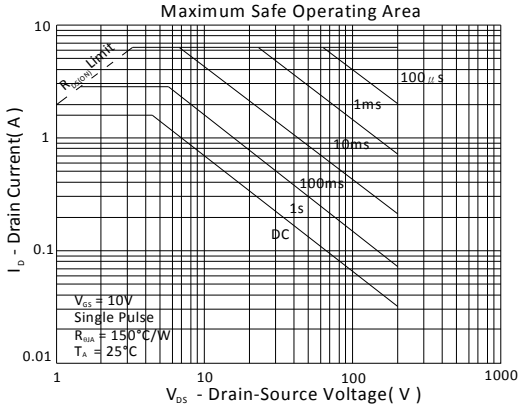
Gate Charge Characteristics



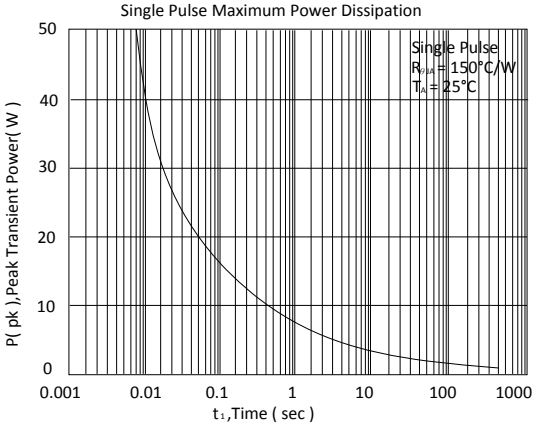
Capacitance Characteristics



Maximum Safe Operating Area



Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve